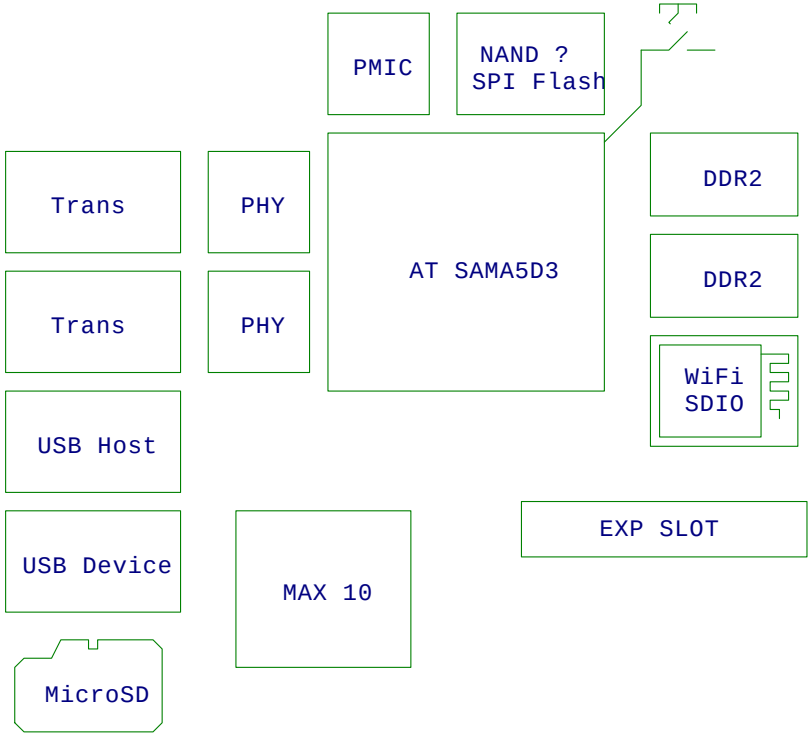
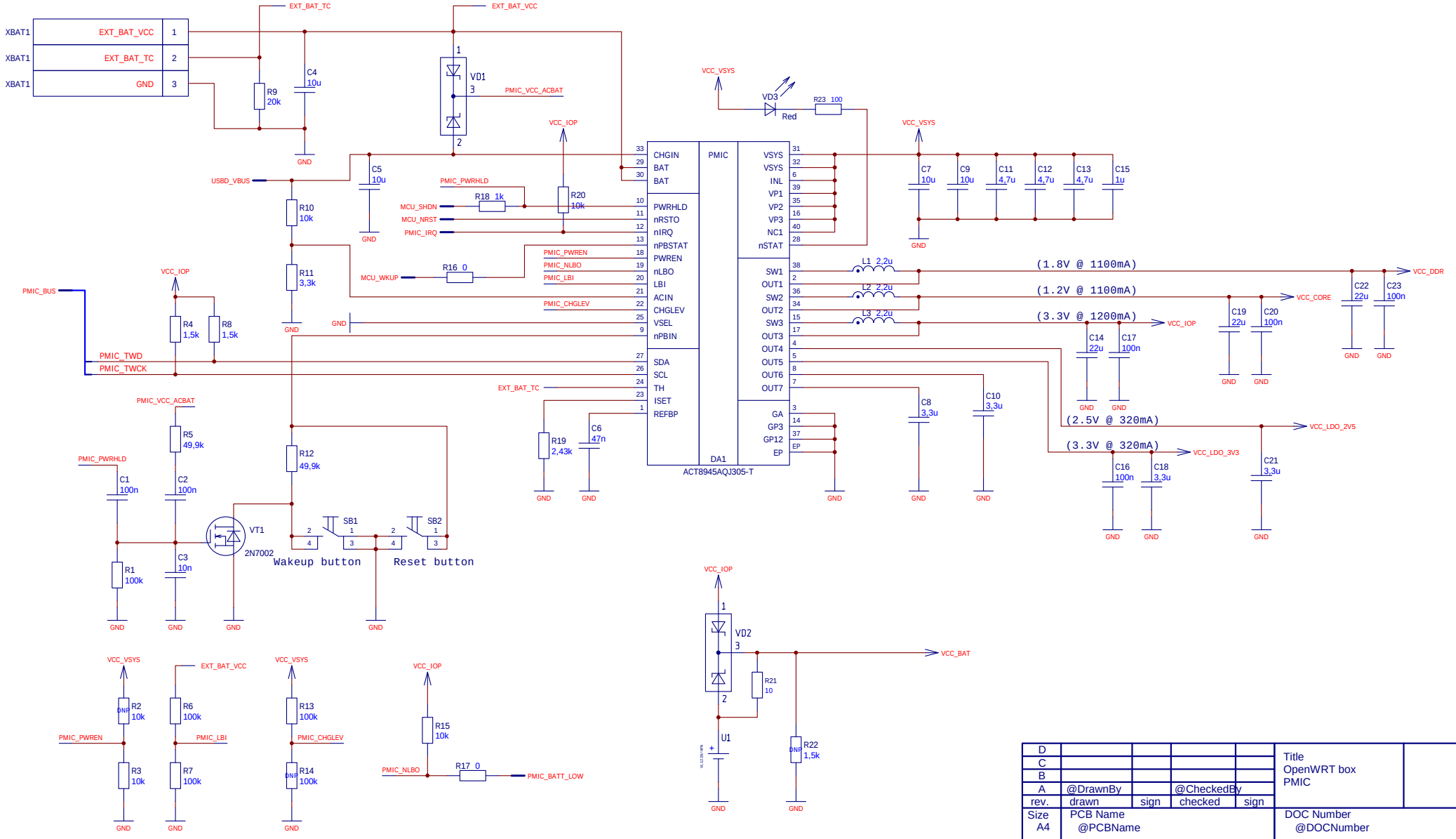
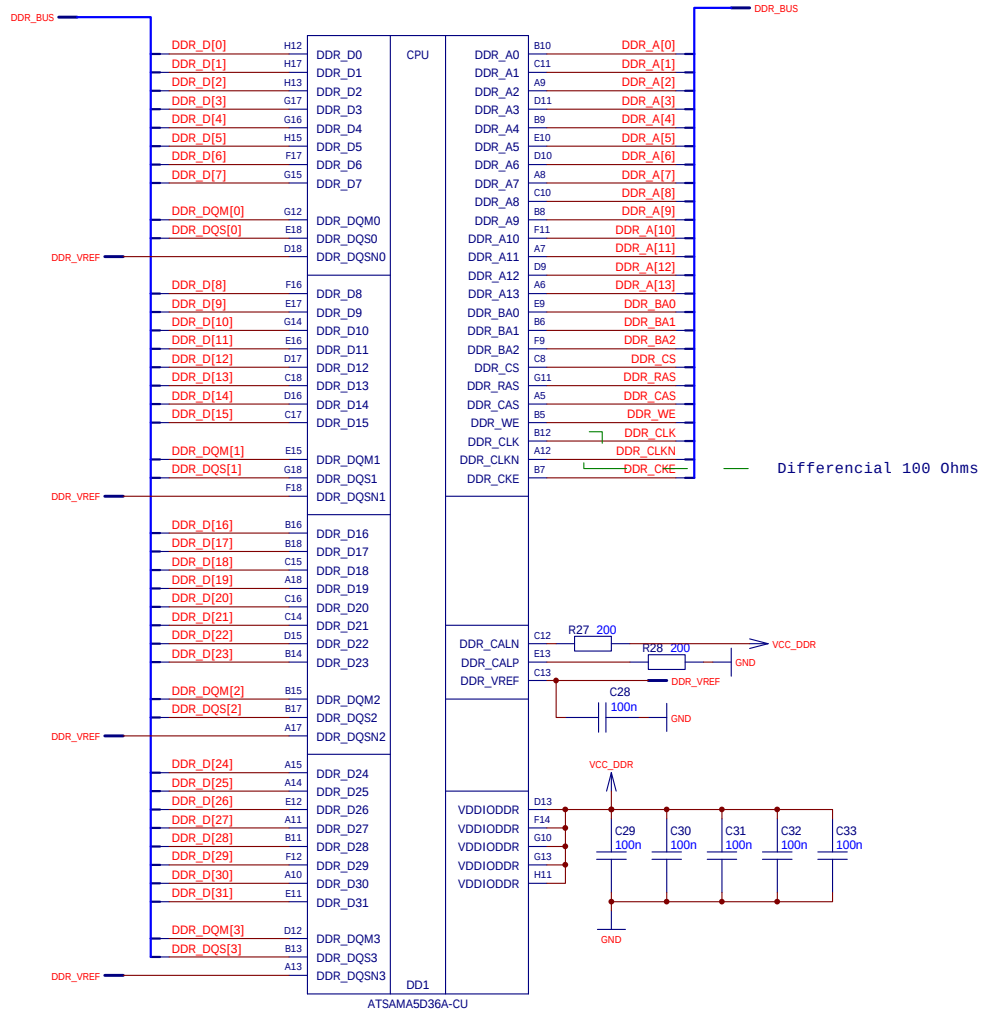


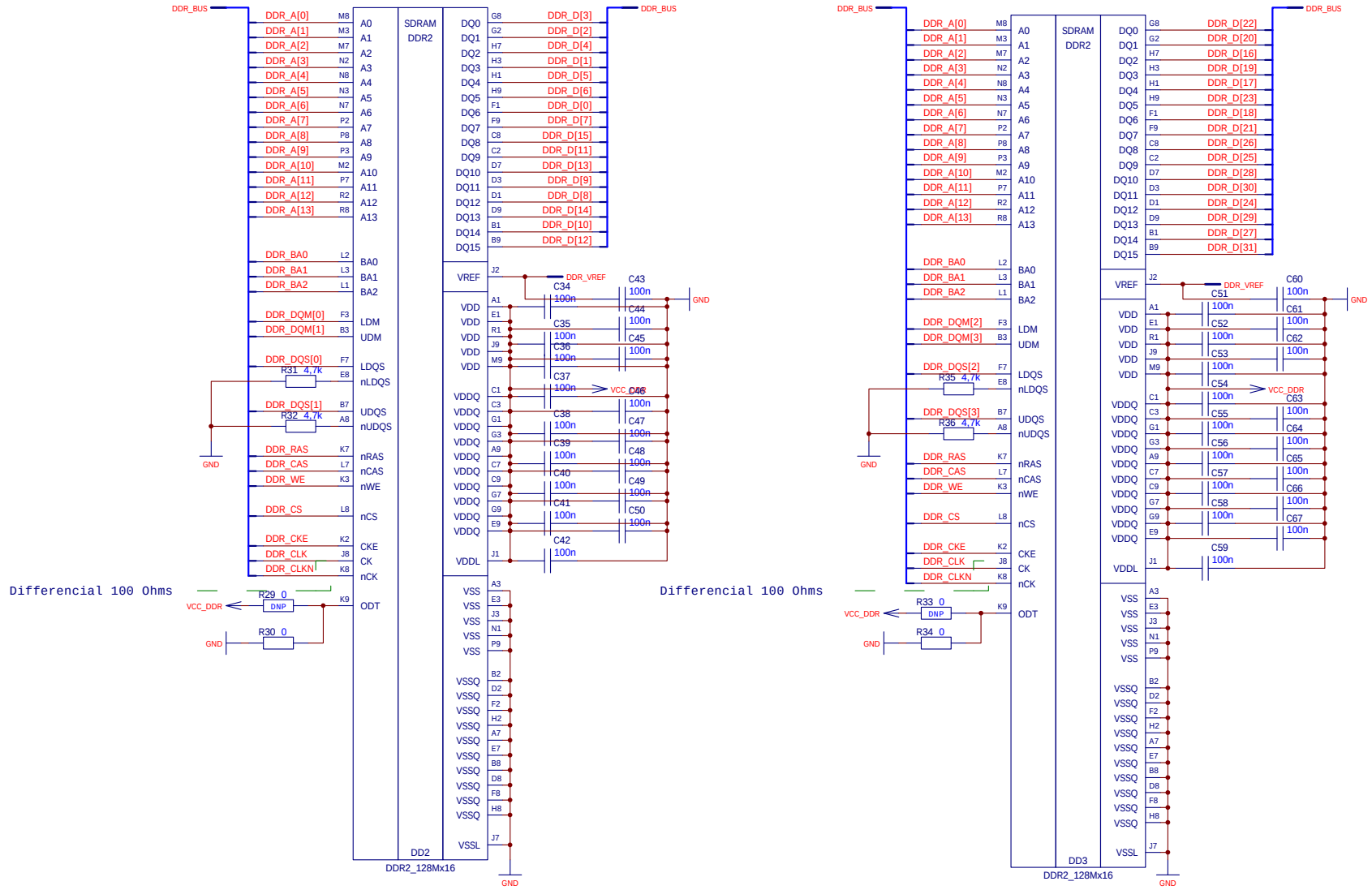
D					Title
C					
B					
A	@DrawnBy		@CheckedBy		
rev.	drawn	sign	checked	sign	
Size A4	PCB Name @PCBName				DOC Number @DOCNumber
Date: 24.01.2016					Page 1 of 17



D					Title: OpenWRT box PMIC
C					
B					
A	@DrawnBy		@CheckedBy		
rev.	drawn	sign	checked	sign	
Size A4	PCB Name @PCBName				DOC Number @DOCNumber
Date: 25.01.2016					Page 2 of 17



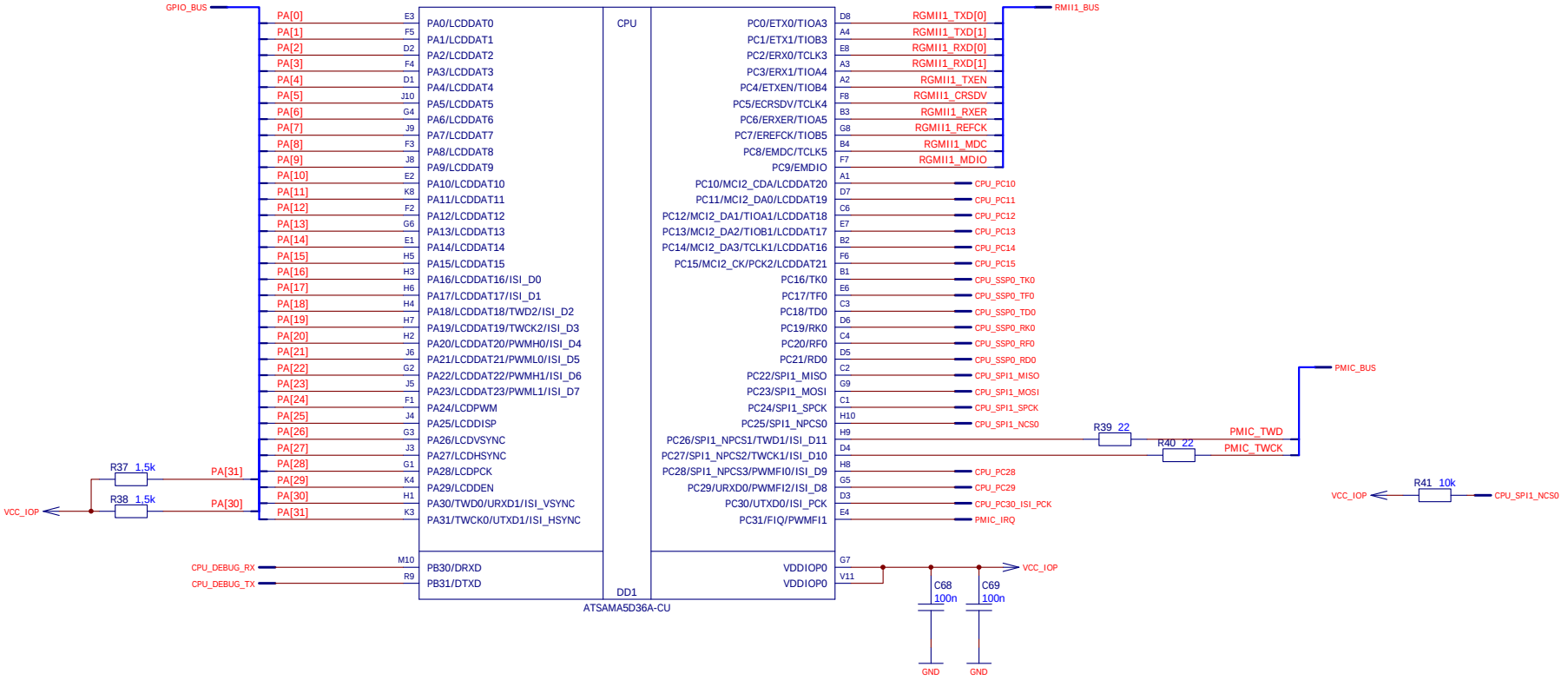
D					Title: OpenWRT box MCU (DDR2)
C					
B					
A	@DrawnBy		@CheckedBy		
rev.	drawn	sign	checked	sign	
Size A4	PCB Name @PCBName				DOC Number @DOCNumber
Date: 25.01.2016					Page 3 of 17



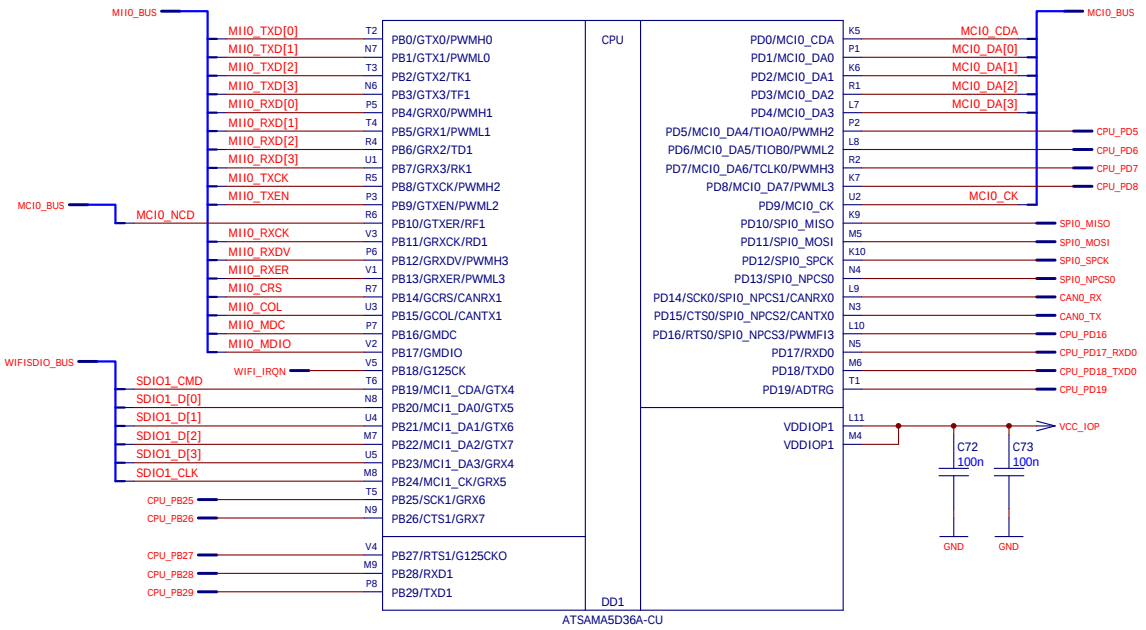
NOTES:
Keep nets as short as possible, therefore, DDR2 devices have to be placed close as possible of SAMA5D36
The layout EBI DDR2 should use controlled impedance traces of Zo= 50ohm characteristic impedance

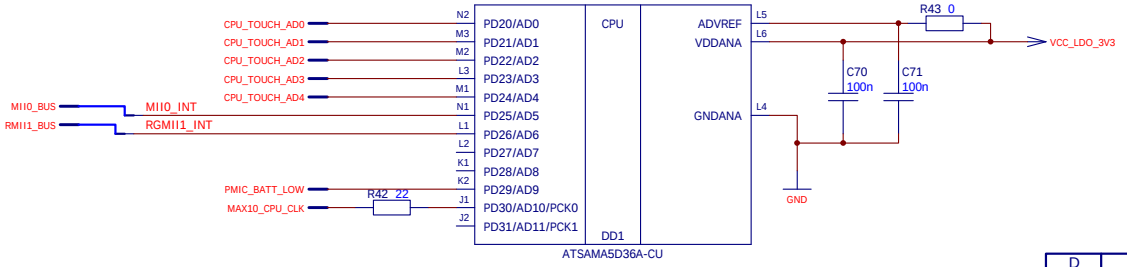
Address, control and data traces may not exceed 1.3 inches (33.0 mm).
Address, control and data traces must be length-matched to within 0.1 inch (2.54mm).
Address, control and data traces must match the data group trace lengths to within 0.25 inches (6.35mm).

D					Title: OpenWRT box DDR2 Memory
C					
B					
A	@DrawnBy		@CheckedBy		
rev.	drawn	sign	checked	sign	
Size A4	PCB Name @PCBName				DOC Number @DOCNumber
Date: 25.01.2016					Page 4 of 17

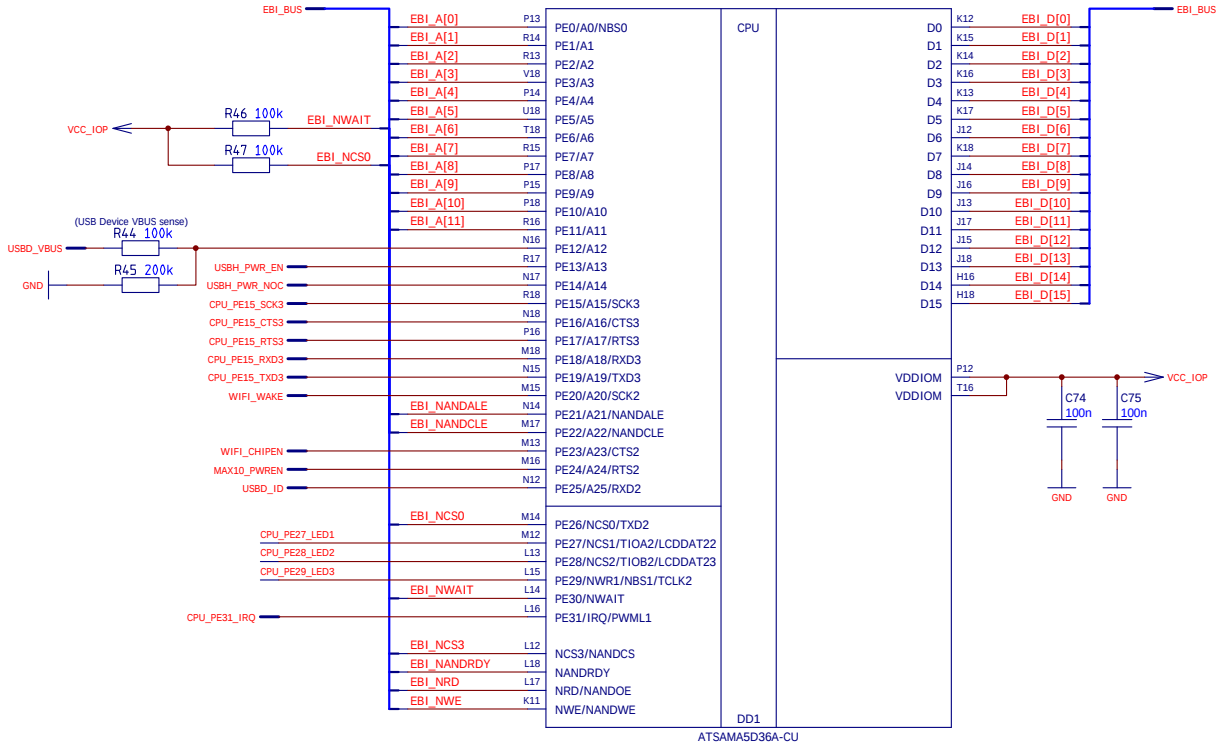


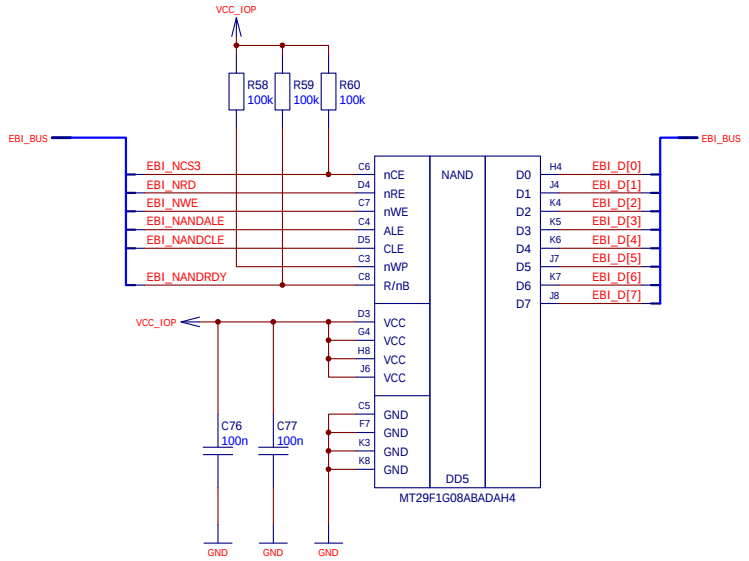
D					Title: OpenWRT box MCU (GPIO p1)
C					
B					
A	@DrawnBy		@CheckedBy		
rev.	drawn	sign	checked	sign	
Size A4	PCB Name @PCBName				DOC Number @DOCNumber
Date: 25.01.2016					Page 5 of 17

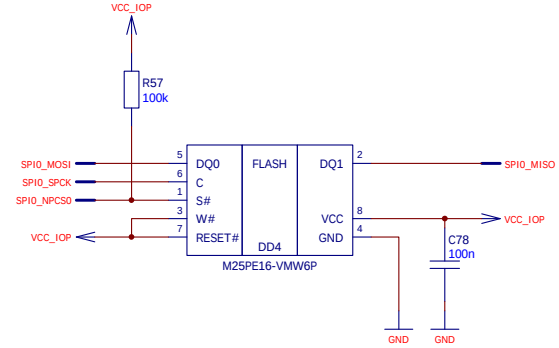


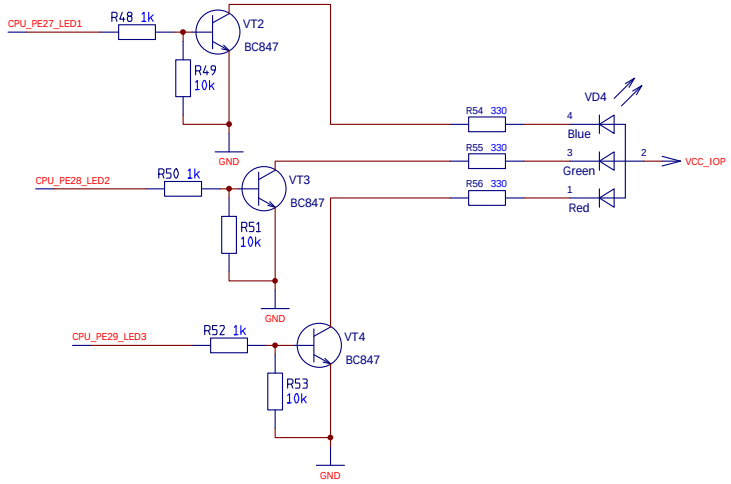


D					Title OpenWRT box MCU (GPIO p2)
C					
B					
A	@DrawnBy		@CheckedBy		
rev.	drawn	sign	checked	sign	
Size A4	PCB Name @PCBName				DOC Number @DOCNumber
	Date: 25.01.2016				Page 6 of 17

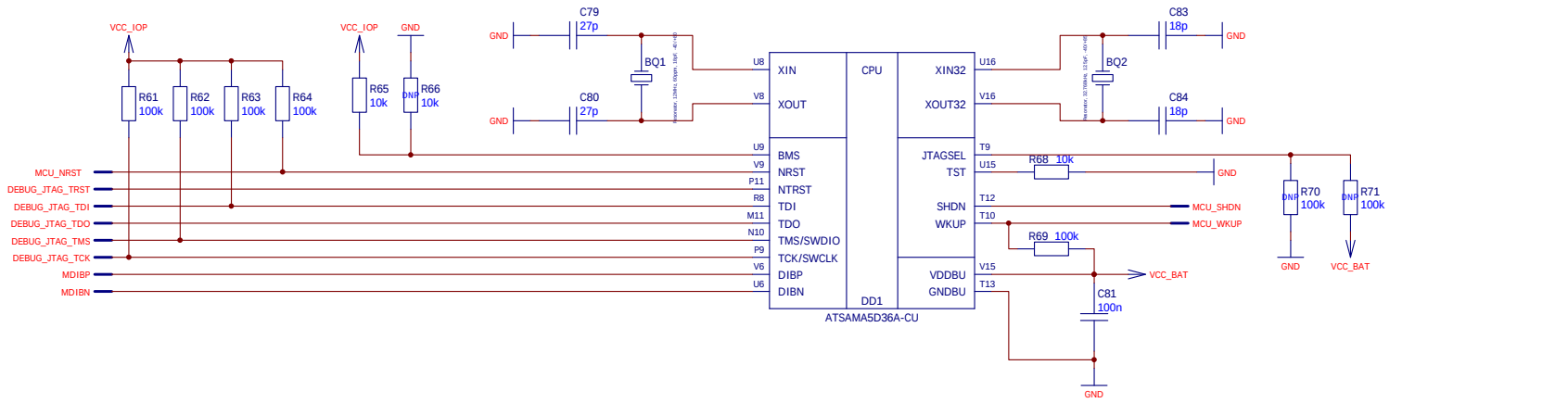


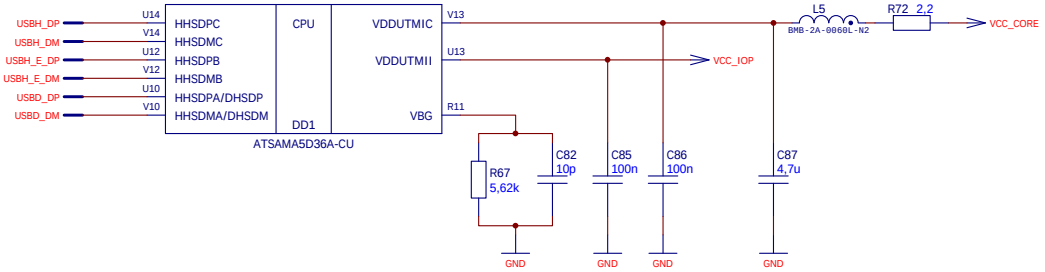




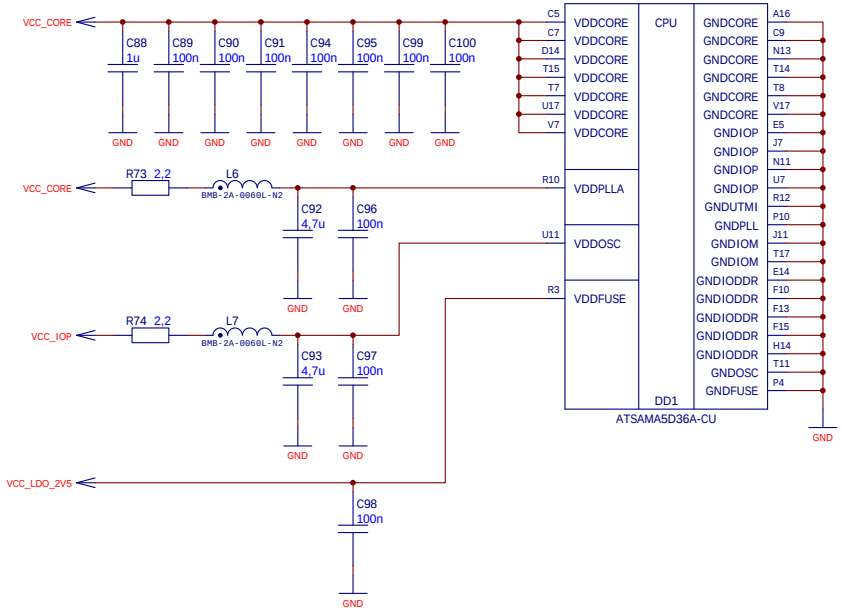


D					Title: OpenWRT box MCU (GPIO p3, Flash memory)
C					
B					
A	@DrawnBy		@CheckedBy		
rev.	drawn	sign	checked	sign	
Size A4	PCB Name @PCBName				DOC Number @DOCNumber
	Date: 25.01.2016				Page 7 of 17

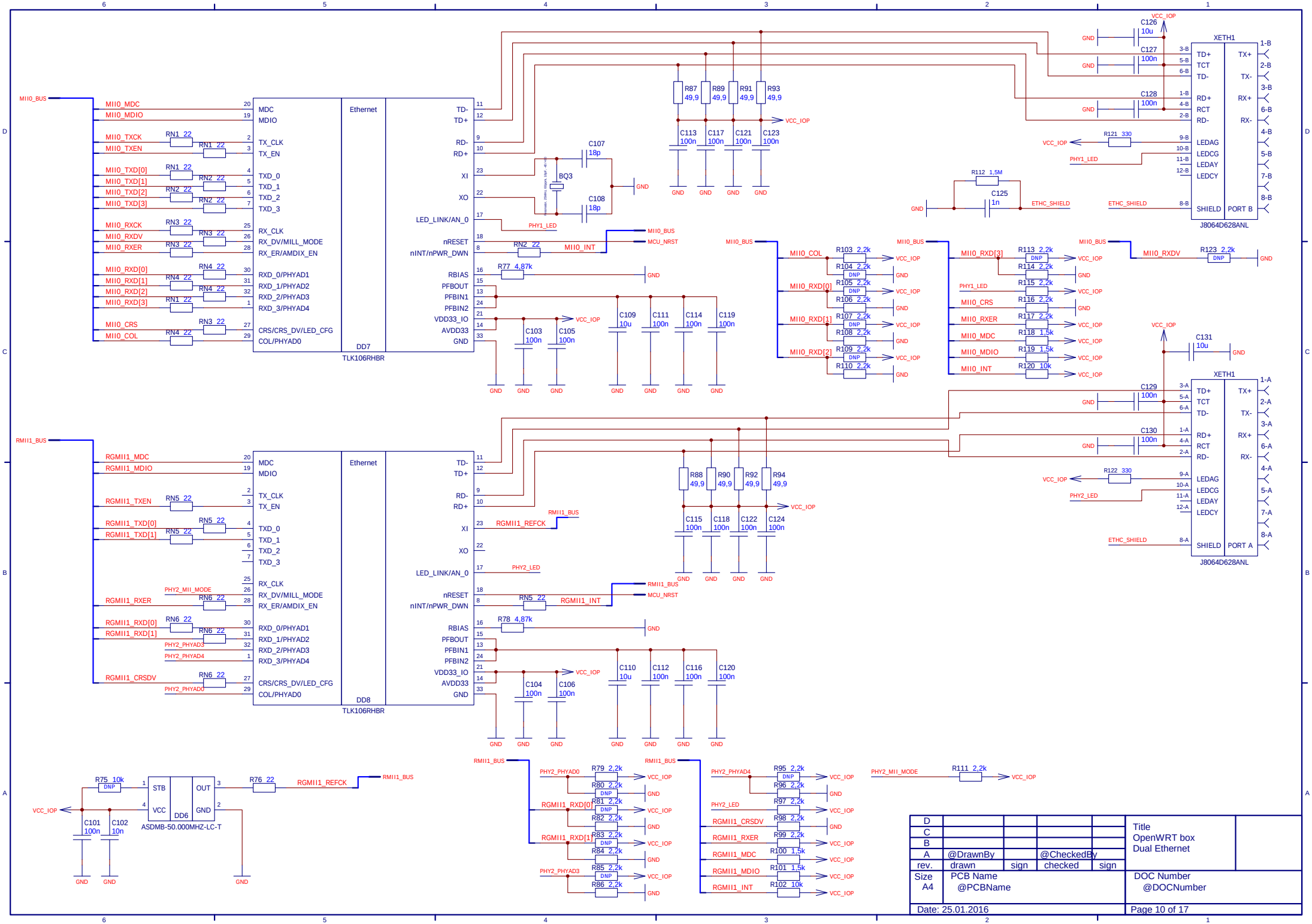


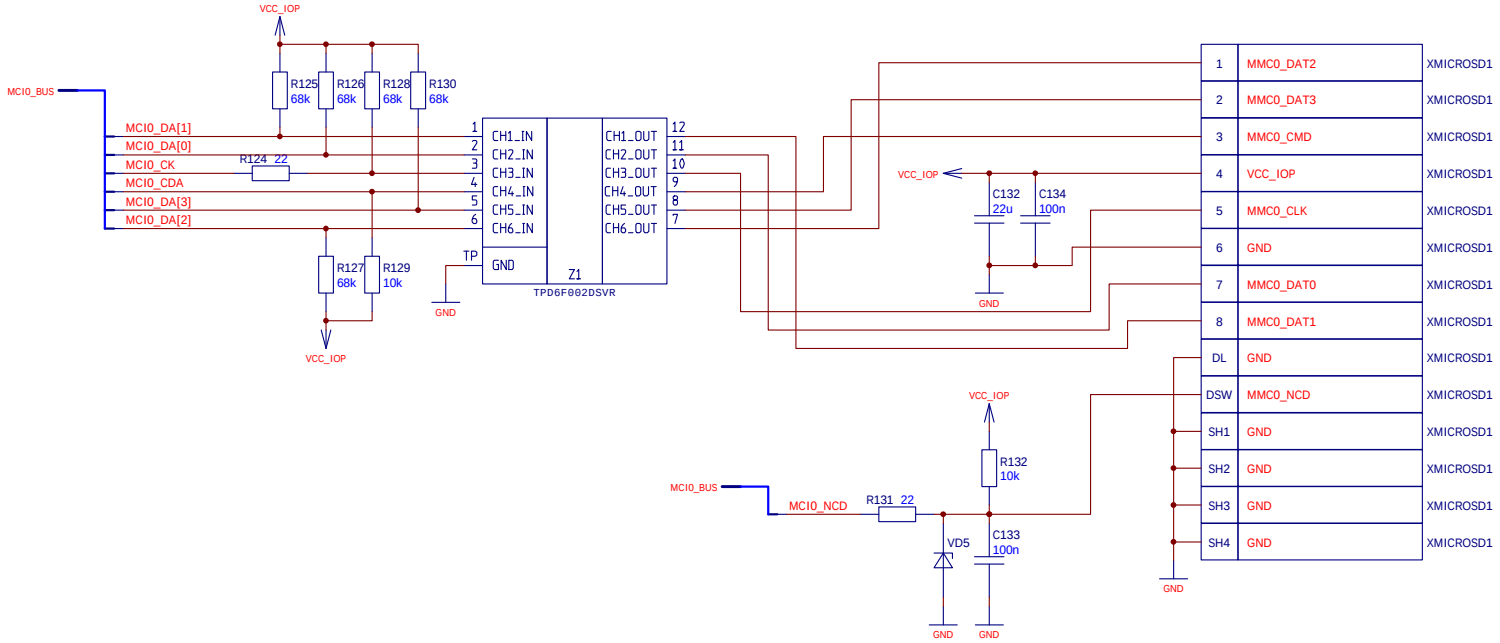


D					Title: OpenWRT box MCU (MISC)
C					
B					
A	@DrawnBy		@CheckedBy		
rev.	drawn	sign	checked	sign	
Size A4	PCB Name @PCBName				DOC Number @DOCNumber
Date: 25.01.2016					Page 8 of 17

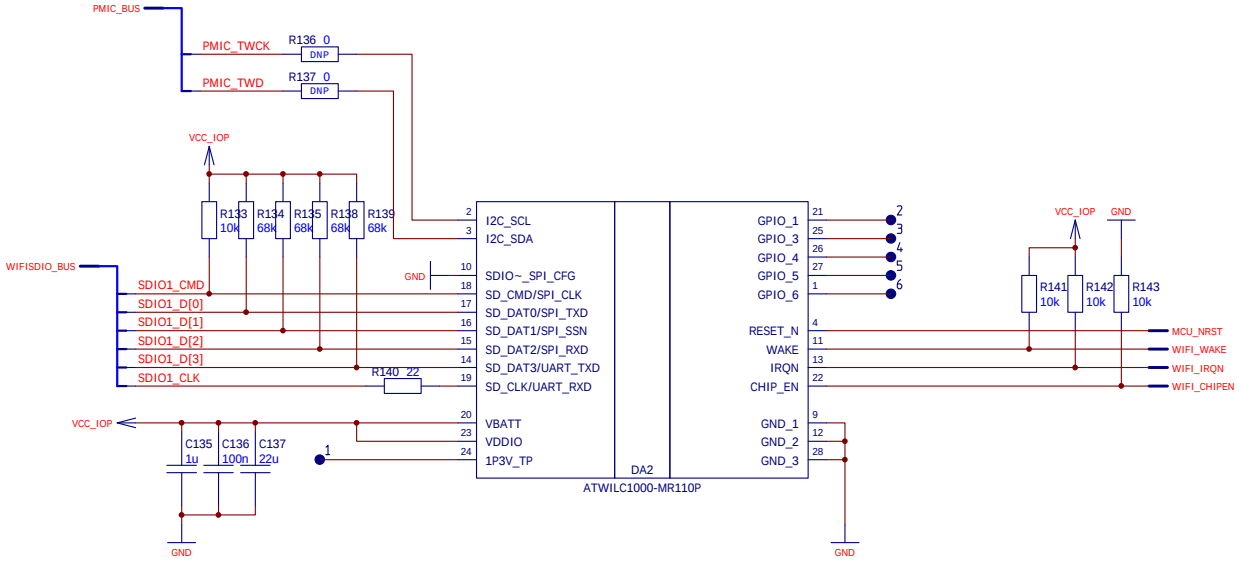


D					Title: OpenWRT box MCU (Power)
C					
B					
A	@DrawnBy		@CheckedBy		
rev.	drawn	sign	checked	sign	
Size A4	PCB Name @PCBName				DOC Number @DOCNumber
Date: 25.01.2016					Page 9 of 17

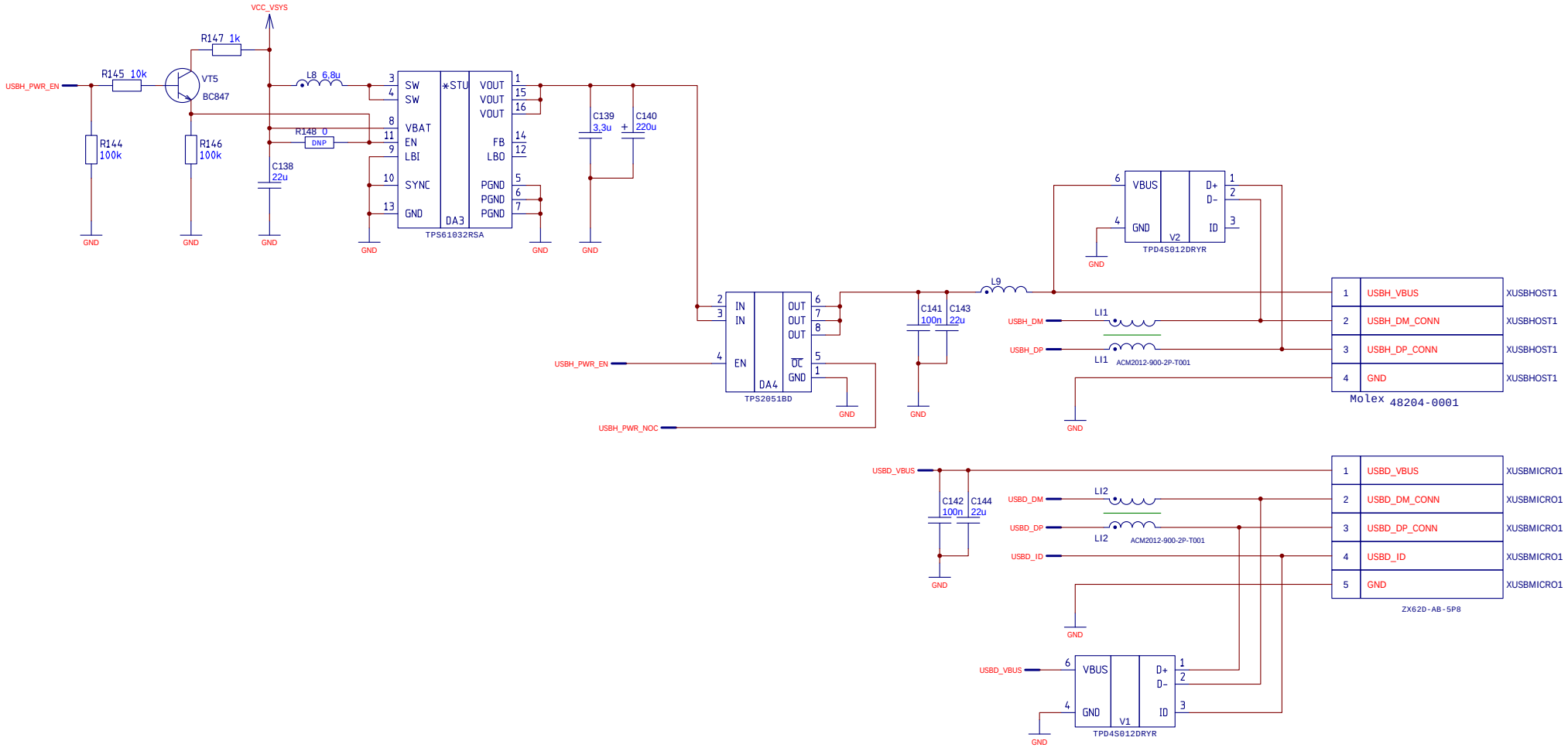

MII0_BUS
MII0_MDC
MII0_MDIO
MII0_TXCK
MII0_TXEN
MII0_TXD[0]
MII0_TXD[1]
MII0_TXD[2]
MII0_TXD[3]
MII0_RXCK
MII0_RXDV
MII0_RXER
MII0_RXD[0]
MII0_RXD[1]
MII0_RXD[2]
MII0_RXD[3]
MII0_CRS
MII0_COL
MDC
MDIO
TX_CLK
TX_EN
TXD_0
TXD_1
TXD_2
TXD_3
RX_CLK
RX_DV/MILL_MODE
RX_ER/AMDIX_EN
RXD_0/PHYAD1
RXD_1/PHYAD2
RXD_2/PHYAD3
RXD_3/PHYAD4
CRS/CRS_DV/LED_CFG
COL/PHYAD0
Ethernet
DD7
TLK106RHBR
TD-
TD+
RD-
RD+
XI
XO
LED_LINK/AN_0
nRESET
nINT/nPWR_DWN
RBIAS
PFBOUT
PFBIN1
PFBIN2
VDD33_IO
AVDD33
GND
MII0_INT
MII0_NRST
R77 4,87k
R87 49,9
R89 49,9
R91 49,9
R93 49,9
C113 100n
C117 100n
C121 100n
C123 100n
C107 18p
C108 18p
BQ3
PHY1_LED
VCC_IOP
C103 100n
C105 100n
C109 10u
C111 100n
C114 100n
C119 100n
XETH1
J8064D628ANL
C126 10u
C127 100n
C128 100n
R121 330
R112 1,5M
C125 1n
ETHC_SHIELD
R103 2,2k
R104 2,2k
R105 2,2k
R106 2,2k
R107 2,2k
R108 2,2k
R109 2,2k
R110 2,2k
R113 2,2k
R114 2,2k
R115 2,2k
R116 2,2k
R117 2,2k
R118 1,5k
R119 1,5k
R120 10k
R123 2,2k
DNP
C131 10u
C129 100n
C130 100n
R122 330
PHY2_LED
RMII1_BUS
RGMII1_MDC
RGMII1_MDIO
RGMII1_TXEN
RGMII1_TXD[0]
RGMII1_TXD[1]
RGMII1_RXER
RGMII1_RXD[0]
RGMII1_RXD[1]
RGMII1_CRSDV
PHY2_MII_MODE
PHY2_PHYAD3
PHY2_PHYAD4
PHY2_PHYAD0
RGMII1_REFCK
RGMII1_INT
R78 4,87k
R88 49,9
R90 49,9
R92 49,9
R94 49,9
C115 100n
C118 100n
C122 100n
C124 100n
C104 100n
C106 100n
C110 10u
C112 100n
C116 100n
C120 100n
R75 10k
R76 22
STB
OUT
VCC
GND
DD6
ASDMB-50.000MHZ-LC-T
C101 100n
C102 10n
R79 2,2k
R80 2,2k
R81 2,2k
R82 2,2k
R83 2,2k
R84 2,2k
R85 2,2k
R86 2,2k
R95 2,2k
R96 2,2k
R97 2,2k
R98 2,2k
R99 2,2k
R100 1,5k
R101 1,5k
R102 10k
R111 2,2k
Title
OpenWRT box
Dual Ethernet
@DrawnBy
@CheckedBy
drawn
checked
sign
Size
A4
PCB Name
@PCBName
DOC Number
@DOCNumber
Date: 25.01.2016
Page 10 of 17



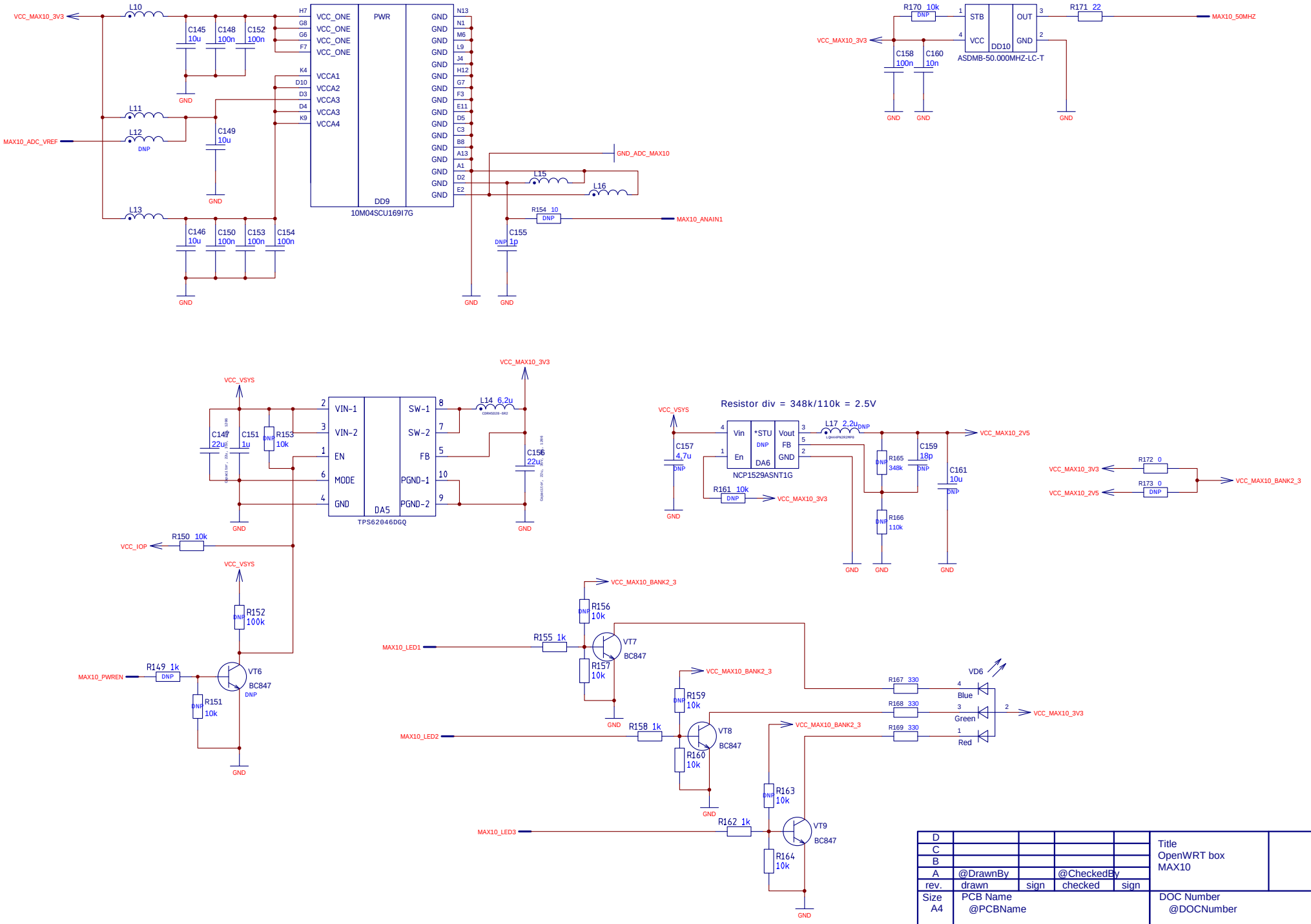
D					Title: OpenWRT box MicroSD slot
C					
B					
A	@DrawnBy		@CheckedBy		
rev.	drawn	sign	checked	sign	
Size A4	PCB Name @PCBName				DOC Number @DOCNumber
Date: 25.01.2016					Page 11 of 17



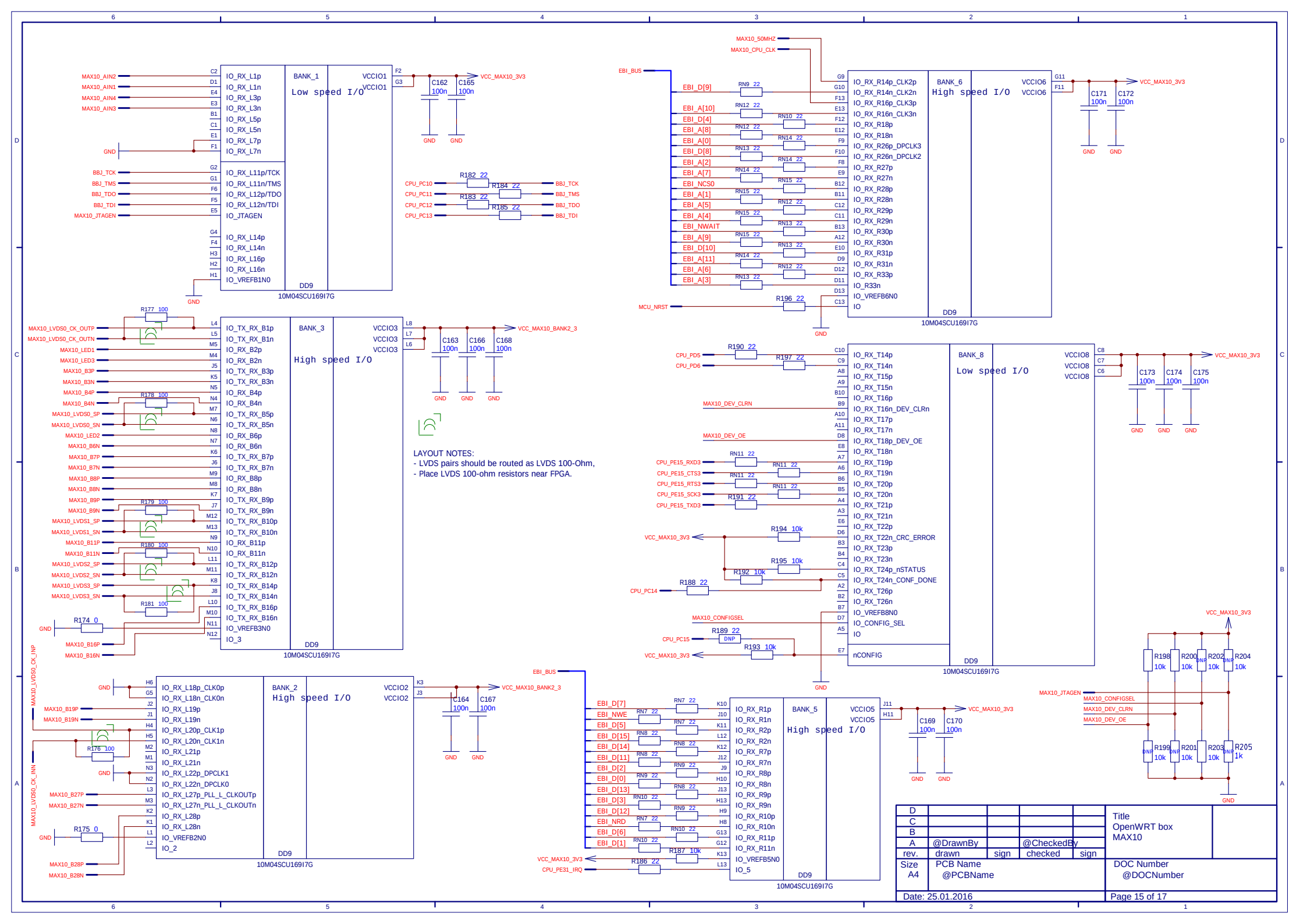
D					Title OpenWRT box WiFi
C					
B					
A	@DrawnBy		@CheckedBy		
rev.	drawn	sign	checked	sign	
Size A4	PCB Name @PCBName				DOC Number @DOCNumber
Date: 25.01.2016					Page 12 of 17

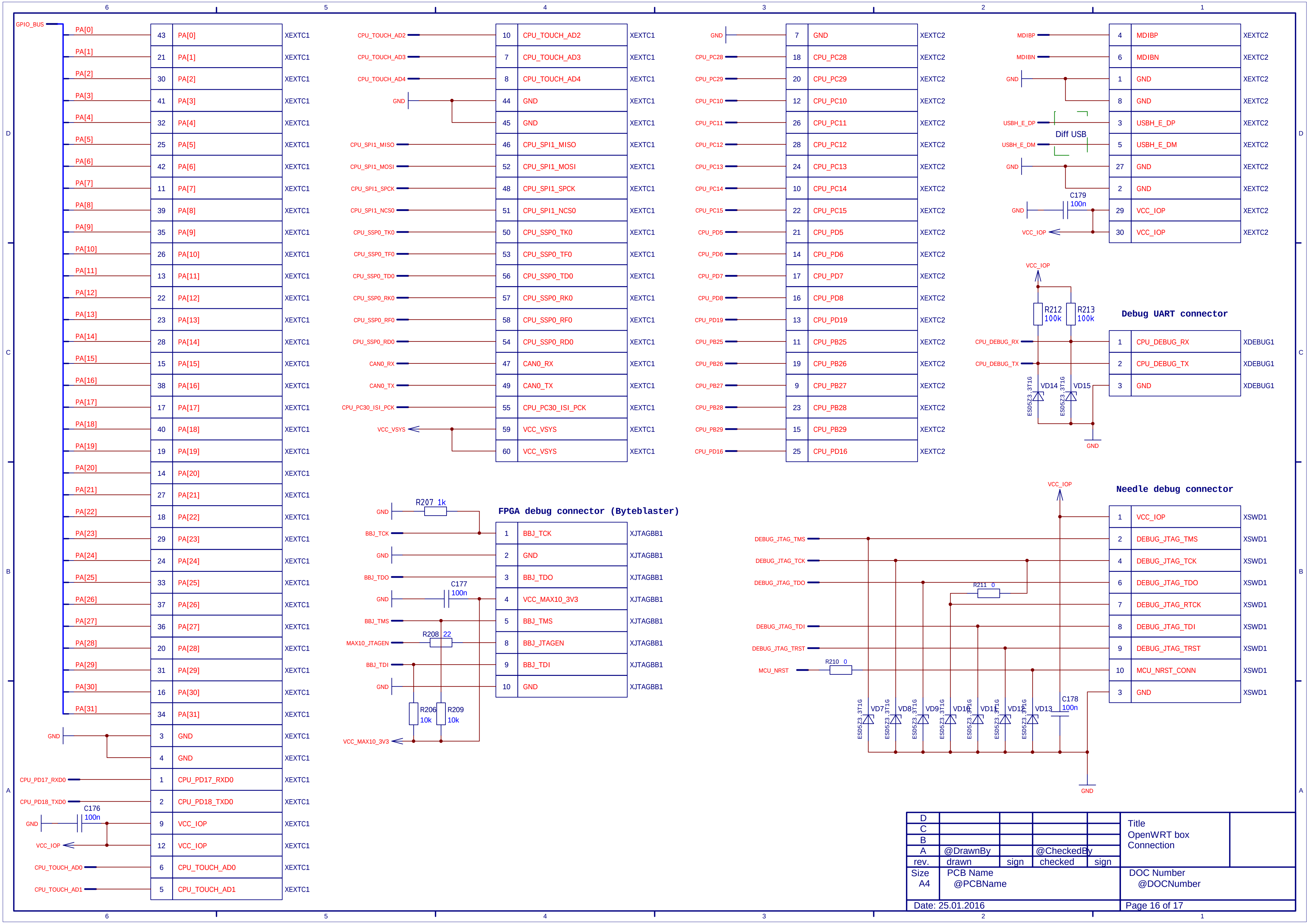


D					Title: OpenWRT box USB
C					
B					
A	@DrawnBy		@CheckedBy		
rev.	drawn	sign	checked	sign	
Size A4	PCB Name @PCBName				DOC Number @DOCNumber
Date: 25.01.2016					Page 13 of 17



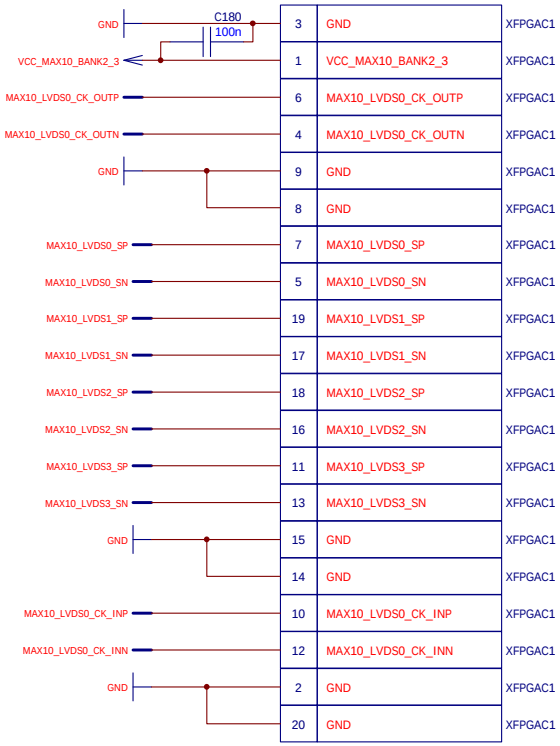
D					Title: OpenWRT box MAX10
C					
B					
A	@DrawnBy		@CheckedBy		
rev.	drawn	sign	checked	sign	
Size A4	PCB Name @PCBName				DOC Number @DOCNumber
Date: 25.01.2016					Page 14 of 17


BANK_1
Low speed I/O
IO_RX_L1p
IO_RX_L1n
IO_RX_L3p
IO_RX_L3n
IO_RX_L5p
IO_RX_L5n
IO_RX_L7p
IO_RX_L7n
IO_RX_L11p/TCK
IO_RX_L11n/TMS
IO_RX_L12p/TDO
IO_RX_L12n/TDI
IO_JTAGEN
IO_RX_L14p
IO_RX_L14n
IO_RX_L16p
IO_RX_L16n
IO_VREFB1N0
VCCIO1
VCCIO1
DD9
10M04SCU169I7G
MAX10_AIN2
MAX10_AIN1
MAX10_AIN4
MAX10_AIN3
GND
BBJ_TCK
BBJ_TMS
BBJ_TDO
BBJ_TDI
MAX10_JTAGEN
C162 100n
C165 100n
VCC_MAX10_3V3
R182 22
R184 22
R183 22
R185 22
CPU_PC10
CPU_PC11
CPU_PC12
CPU_PC13
BANK_6
High speed I/O
IO_RX_R14p_CLK2p
IO_RX_R14n_CLK2n
IO_RX_R16p_CLK3p
IO_RX_R16n_CLK3n
IO_RX_R18p
IO_RX_R18n
IO_RX_R26p_DPCLK3
IO_RX_R26n_DPCLK2
IO_RX_R27p
IO_RX_R27n
IO_RX_R28p
IO_RX_R28n
IO_RX_R29p
IO_RX_R29n
IO_RX_R30p
IO_RX_R30n
IO_RX_R31p
IO_RX_R31n
IO_R33p
IO_R33n
IO_VREFB6N0
IO
VCCIO6
VCCIO6
MAX10_50MHZ
MAX10_CPU_CLK
EBI_BUS
EBI_D[9]
EBI_A[10]
EBI_D[4]
EBI_A[8]
EBI_A[0]
EBI_D[8]
EBI_A[2]
EBI_A[7]
EBI_NCS0
EBI_A[1]
EBI_A[5]
EBI_A[4]
EBI_NWAIT
EBI_A[9]
EBI_D[10]
EBI_A[11]
EBI_A[6]
EBI_A[3]
MCU_NRST
R196 22
C171 100n
C172 100n
BANK_3
High speed I/O
IO_TX_RX_B1p
IO_TX_RX_B1n
IO_RX_B2p
IO_RX_B2n
IO_TX_RX_B3p
IO_TX_RX_B3n
IO_RX_B4p
IO_RX_B4n
IO_TX_RX_B5p
IO_TX_RX_B5n
IO_RX_B6p
IO_RX_B6n
IO_TX_RX_B7p
IO_TX_RX_B7n
IO_RX_B8p
IO_RX_B8n
IO_TX_RX_B9p
IO_TX_RX_B9n
IO_TX_RX_B10p
IO_TX_RX_B10n
IO_RX_B11p
IO_RX_B11n
IO_TX_RX_B12p
IO_TX_RX_B12n
IO_TX_RX_B14p
IO_TX_RX_B14n
IO_TX_RX_B16p
IO_TX_RX_B16n
IO_VREFB3N0
IO_3
VCCIO3
VCCIO3
VCCIO3
MAX10_LVDS0_CK_OUTP
MAX10_LVDS0_CK_OUTN
MAX10_LED1
MAX10_LED3
MAX10_B3P
MAX10_B3N
MAX10_B4P
MAX10_B4N
MAX10_LVDS0_SP
MAX10_LVDS0_SN
MAX10_LED2
MAX10_B6N
MAX10_B7P
MAX10_B7N
MAX10_B8P
MAX10_B8N
MAX10_B9P
MAX10_B9N
MAX10_LVDS1_SP
MAX10_LVDS1_SN
MAX10_B11P
MAX10_B11N
MAX10_LVDS2_SP
MAX10_LVDS2_SN
MAX10_LVDS3_SP
MAX10_LVDS3_SN
MAX10_B16P
MAX10_B16N
R177 100
R178 100
R179 100
R180 100
R181 100
R174 0
C163 100n
C166 100n
C168 100n
VCC_MAX10_BANK2_3
LAYOUT NOTES:
- LVDS pairs should be routed as LVDS 100-Ohm,
- Place LVDS 100-ohm resistors near FPGA.
BANK_8
Low speed I/O
IO_RX_T14p
IO_RX_T14n
IO_RX_T15p
IO_RX_T15n
IO_RX_T16p
IO_RX_T16n_DEV_CLRn
IO_RX_T17p
IO_RX_T17n
IO_RX_T18p_DEV_OE
IO_RX_T18n
IO_RX_T19p
IO_RX_T19n
IO_RX_T20p
IO_RX_T20n
IO_RX_T21p
IO_RX_T21n
IO_RX_T22p
IO_RX_T22n_CRC_ERROR
IO_RX_T23p
IO_RX_T23n
IO_RX_T24p_nSTATUS
IO_RX_T24n_CONF_DONE
IO_RX_T26p
IO_RX_T26n
IO_VREFB8N0
IO_CONFIG_SEL
IO
nCONFIG
VCCIO8
VCCIO8
VCCIO8
CPU_PD5
CPU_PD6
MAX10_DEV_CLRN
MAX10_DEV_OE
CPU_PE15_RXD3
CPU_PE15_CTS3
CPU_PE15_RTS3
CPU_PE15_SCK3
CPU_PE15_TXD3
R190 22
R197 22
R191 22
R194 10k
R195 10k
R192 10k
R188 22
CPU_PC14
MAX10_CONFIGSEL
R189 22
DNP
CPU_PC15
R193 10k
C173 100n
C174 100n
C175 100n
BANK_2
High speed I/O
IO_RX_L18p_CLK0p
IO_RX_L18n_CLK0n
IO_RX_L19p
IO_RX_L19n
IO_RX_L20p_CLK1p
IO_RX_L20n_CLK1n
IO_RX_L21p
IO_RX_L21n
IO_RX_L22p_DPCLK1
IO_RX_L22n_DPCLK0
IO_RX_L27p_PLL_L_CLKOUTp
IO_RX_L27n_PLL_L_CLKOUTn
IO_RX_L28p
IO_RX_L28n
IO_VREFB2N0
IO_2
VCCIO2
VCCIO2
MAX10_LVDS0_CK_INP
MAX10_LVDS0_CK_INN
MAX10_B19P
MAX10_B19N
MAX10_B27P
MAX10_B27N
MAX10_B28P
MAX10_B28N
R176 100
R175 0
C164 100n
C167 100n
BANK_5
High speed I/O
IO_RX_R1p
IO_RX_R1n
IO_RX_R2p
IO_RX_R2n
IO_RX_R7p
IO_RX_R7n
IO_RX_R8p
IO_RX_R8n
IO_RX_R9p
IO_RX_R9n
IO_RX_R10p
IO_RX_R10n
IO_RX_R11p
IO_RX_R11n
IO_VREFB5N0
IO_5
VCCIO5
VCCIO5
EBI_D[7]
EBI_NWE
EBI_D[5]
EBI_D[15]
EBI_D[14]
EBI_D[11]
EBI_D[2]
EBI_D[0]
EBI_D[13]
EBI_D[3]
EBI_D[12]
EBI_NRD
EBI_D[6]
EBI_D[1]
R187 10k
R186 22
CPU_PE31_IRQ
C169 100n
C170 100n
R198 10k
R200 10k
R202 10k
R204 10k
R199 10k
R201 10k
R203 10k
R205 1k
MAX10_JTAGEN
MAX10_CONFIGSEL
MAX10_DEV_CLRN
MAX10_DEV_OE
D
C
B
A
@DrawnBy
@CheckedBy
rev.
drawn
sign
checked
sign
Size
A4
PCB Name
@PCBName
Title
OpenWRT box
MAX10
DOC Number
@DOCNumber
Date: 25.01.2016
Page 15 of 17



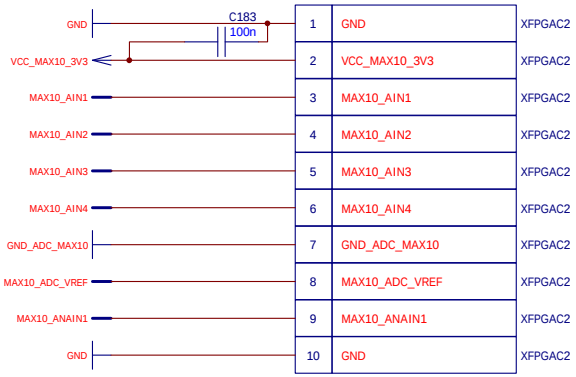
GPIO_BUS
PA[0] PA[1] PA[2] PA[3] PA[4] PA[5] PA[6] PA[7] PA[8] PA[9] PA[10] PA[11] PA[12] PA[13] PA[14] PA[15] PA[16] PA[17] PA[18] PA[19] PA[20] PA[21] PA[22] PA[23] PA[24] PA[25] PA[26] PA[27] PA[28] PA[29] PA[30] PA[31]
XEXTC1
43 PA[0]
21 PA[1]
30 PA[2]
41 PA[3]
32 PA[4]
25 PA[5]
42 PA[6]
11 PA[7]
39 PA[8]
35 PA[9]
26 PA[10]
13 PA[11]
22 PA[12]
23 PA[13]
28 PA[14]
15 PA[15]
38 PA[16]
17 PA[17]
40 PA[18]
19 PA[19]
14 PA[20]
27 PA[21]
18 PA[22]
29 PA[23]
24 PA[24]
33 PA[25]
37 PA[26]
36 PA[27]
20 PA[28]
31 PA[29]
16 PA[30]
34 PA[31]
3 GND
4 GND
1 CPU_PD17_RXD0
2 CPU_PD18_TXD0
9 VCC_IOP
12 VCC_IOP
6 CPU_TOUCH_AD0
5 CPU_TOUCH_AD1
C176 100n
10 CPU_TOUCH_AD2
7 CPU_TOUCH_AD3
8 CPU_TOUCH_AD4
44 GND
45 GND
46 CPU_SPI1_MISO
52 CPU_SPI1_MOSI
48 CPU_SPI1_SPCK
51 CPU_SPI1_NCS0
50 CPU_SSP0_TK0
53 CPU_SSP0_TF0
56 CPU_SSP0_TD0
57 CPU_SSP0_RK0
58 CPU_SSP0_RF0
54 CPU_SSP0_RD0
47 CAN0_RX
49 CAN0_TX
55 CPU_PC30_ISI_PCK
59 VCC_VSYS
60 VCC_VSYS
XEXTC2
7 GND
18 CPU_PC28
20 CPU_PC29
12 CPU_PC10
26 CPU_PC11
28 CPU_PC12
24 CPU_PC13
10 CPU_PC14
22 CPU_PC15
21 CPU_PD5
14 CPU_PD6
17 CPU_PD7
16 CPU_PD8
13 CPU_PD19
11 CPU_PB25
19 CPU_PB26
9 CPU_PB27
23 CPU_PB28
15 CPU_PB29
25 CPU_PD16
4 MDIBP
6 MDIBN
1 GND
8 GND
3 USBH_E_DP
5 USBH_E_DM
27 GND
2 GND
29 VCC_IOP
30 VCC_IOP
Diff USB
C179 100n
Debug UART connector
XDEBUG1
1 CPU_DEBUG_RX
2 CPU_DEBUG_TX
3 GND
R212 100k
R213 100k
VD14 VD15 ESD5Z3.3T1G
FPGA debug connector (Byteblaster)
XJTAGBB1
1 BBJ_TCK
2 GND
3 BBJ_TDO
4 VCC_MAX10_3V3
5 BBJ_TMS
8 BBJ_JTAGEN
9 BBJ_TDI
10 GND
R207 1k
C177 100n
R208 22
R206 10k
R209 10k
MAX10_JTAGEN
VCC_MAX10_3V3
Needle debug connector
XSWD1
1 VCC_IOP
2 DEBUG_JTAG_TMS
4 DEBUG_JTAG_TCK
6 DEBUG_JTAG_TDO
7 DEBUG_JTAG_RTCK
8 DEBUG_JTAG_TDI
9 DEBUG_JTAG_TRST
10 MCU_NRST_CONN
3 GND
R211 0
R210 0
MCU_NRST
VD7 VD8 VD9 VD10 VD11 VD12 VD13 ESD5Z3.3T1G
C178 100n
Title
OpenWRT box
Connection
rev. drawn sign checked sign
A @DrawnBy @CheckedBy
Size A4
PCB Name @PCBName
DOC Number @DOCNumber
Date: 25.01.2016
Page 16 of 17

FPGA LVDS port



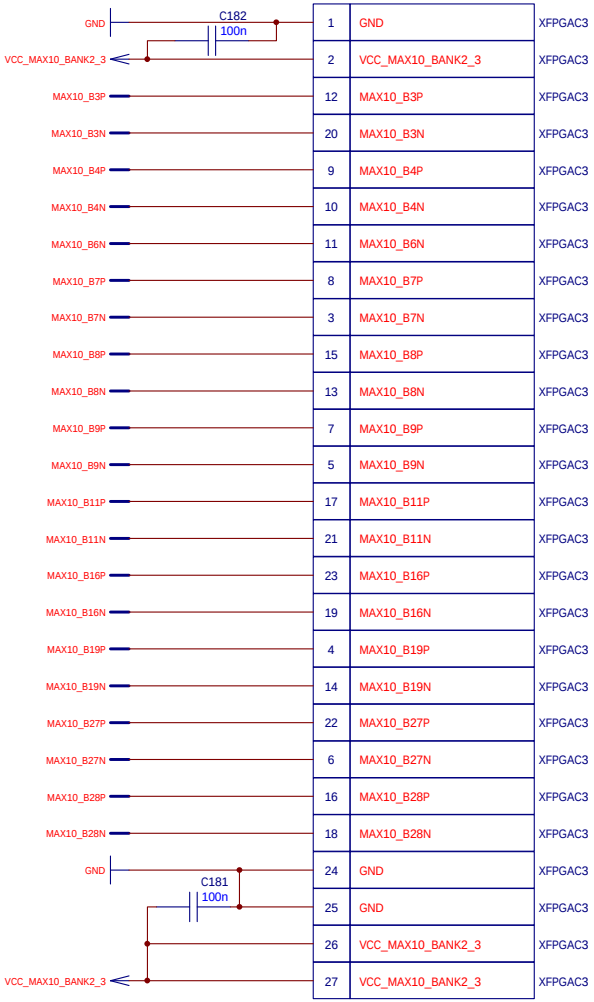
3	GND	XFPGAC1
1	VCC_MAX10_BANK2_3	XFPGAC1
6	MAX10_LVDS0_CK_OUTP	XFPGAC1
4	MAX10_LVDS0_CK_OUTN	XFPGAC1
9	GND	XFPGAC1
8	GND	XFPGAC1
7	MAX10_LVDS0_SP	XFPGAC1
5	MAX10_LVDS0_SN	XFPGAC1
19	MAX10_LVDS1_SP	XFPGAC1
17	MAX10_LVDS1_SN	XFPGAC1
18	MAX10_LVDS2_SP	XFPGAC1
16	MAX10_LVDS2_SN	XFPGAC1
11	MAX10_LVDS3_SP	XFPGAC1
13	MAX10_LVDS3_SN	XFPGAC1
15	GND	XFPGAC1
14	GND	XFPGAC1
10	MAX10_LVDS0_CK_INP	XFPGAC1
12	MAX10_LVDS0_CK_INN	XFPGAC1
2	GND	XFPGAC1
20	GND	XFPGAC1

FPGA analog port



1	GND	XFPGAC2
2	VCC_MAX10_3V3	XFPGAC2
3	MAX10_AIN1	XFPGAC2
4	MAX10_AIN2	XFPGAC2
5	MAX10_AIN3	XFPGAC2
6	MAX10_AIN4	XFPGAC2
7	GND_ADC_MAX10	XFPGAC2
8	MAX10_ADC_VREF	XFPGAC2
9	MAX10_ANAIN1	XFPGAC2
10	GND	XFPGAC2

FPGA I/O port



1	GND	XFPGAC3
2	VCC_MAX10_BANK2_3	XFPGAC3
12	MAX10_B3P	XFPGAC3
20	MAX10_B3N	XFPGAC3
9	MAX10_B4P	XFPGAC3
10	MAX10_B4N	XFPGAC3
11	MAX10_B6N	XFPGAC3
8	MAX10_B7P	XFPGAC3
3	MAX10_B7N	XFPGAC3
15	MAX10_B8P	XFPGAC3
13	MAX10_B8N	XFPGAC3
7	MAX10_B9P	XFPGAC3
5	MAX10_B9N	XFPGAC3
17	MAX10_B11P	XFPGAC3
21	MAX10_B11N	XFPGAC3
23	MAX10_B16P	XFPGAC3
19	MAX10_B16N	XFPGAC3
4	MAX10_B19P	XFPGAC3
14	MAX10_B19N	XFPGAC3
22	MAX10_B27P	XFPGAC3
6	MAX10_B27N	XFPGAC3
16	MAX10_B28P	XFPGAC3
18	MAX10_B28N	XFPGAC3
24	GND	XFPGAC3
25	GND	XFPGAC3
26	VCC_MAX10_BANK2_3	XFPGAC3
27	VCC_MAX10_BANK2_3	XFPGAC3

D					Title OpenWRT box Connection (FPGA)
C					
B					
A	@DrawnBy		@CheckedBy		
rev.	drawn	sign	checked	sign	
Size A4	PCB Name @PCBName				DOC Number @DOCNumber
	Date: 25.01.2016				Page 17 of 17